Indian Maritime University

(A Central University, Govt of India)

May-June 2018 End Semester Examinations

B Sc (Nautical Science)

Semester-IV

Nautical Electronics-IV (UG21T2405)

Duration:3 Hrs | Max Marks:70 Marks

Date: 13.06.2018 | Pass Marks:35 Marks

Part A (7 × 10 = 70 Marks)
Answer any seven of the following

1. (a) Implement AND, OR and NOT gate by using NOR gate. (5)

   (b) Demonstrate the validity of DeMorgan's theorem for three variables: $\overline{(x + y + z)} = \bar{x}\bar{y}\bar{z}$ *and* $\overline{(xyz)} = \bar{x} + \bar{y} + \bar{z}$ (5)

2. (a) Simplify the following Boolean expression to a minimum number of literals: $(x + y + \bar{z})(\bar{x} + \bar{y} + z)$ (5)

   (b) Draw logic diagrams of the circuits that implement the original and simplified expressionsin question 2 (a). (5)

3. (a) Draw the multiple-level NAND circuit for the following expression:

   $w(x + y + z) + xyz$ (5)

   (b) Develop the Boolean equation for sum and carry of half adder circuit. Implement the obtained Boolean equations by logic gates. (5)

4. (a) Draw the pin diagram of IC 555. What are applications of IC 555? (5)

   (b) Differentiate Bistable and Monostable operation. (5)

5. (a) Construct SR latch by using NAND gate. Explain its operation. (5)

   (b) Draw and explain the operation of JK flipflop. (5)

6. (a) Construct 4 – Bit binary Ripple Counter using T flipflop and show the truth table. (5)

(b) Construct BCD counter using JK flipflop and show the state diagram. (5)

7. (a) Define Interrupts in 8085 processor and list the types. (5)

(b) Discuss programming model of 8085 processor. (5)

8. Draw pin diagram and an internal architecture of 8085 microprocessor. (10)

9. (a) Implement a full adder with two 4 × 1 multiplexers. (5)

(b) Implement the following Boolean function with a 4 × 1 multiplexer and external gates. $F\ (A, B, C, D)\ =\ \sum(1, 3, 4, 11, 12, 13, 14, 15)$ (5)